# HEF4050B

## Hex non-inverting buffers

Rev. 10 — 23 June 2016 Product data sheet

## 1. General description

The HEF4050B provides six non-inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in Table 3.

It operates over a recommended $V_{DD}$ power supply range of 3 V to 15 V referenced to $V_{SS}$ (usually ground). Unused inputs must be connected to $V_{DD}$, $V_{SS}$, or another input.

## 2. Features and benefits

- Accepts input voltages in excess of the supply voltage
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from −40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

## 3. Applications

- LOCMOS (Local Oxidation CMOS) to DTL/TTL converter
- HIGH sink current for driving two TTL loads
- HIGH-to-LOW level logic conversion

## 4. Ordering information

**Table 1. Ordering information**

*All types operate from −40 °C to +85 °C.*

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| HEF4050BT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |

## 5. Functional diagram

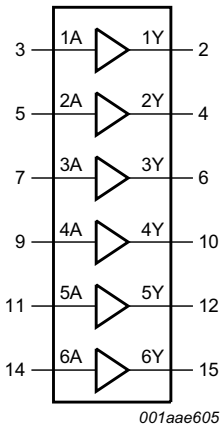



**Fig 1. Logic symbol**

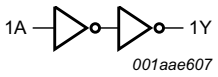



**Fig 2. Logic diagram for one gate**

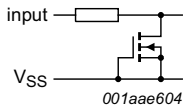



**Fig 3. Input protection circuit**

# 6. Pinning information

## 6.1 Pinning

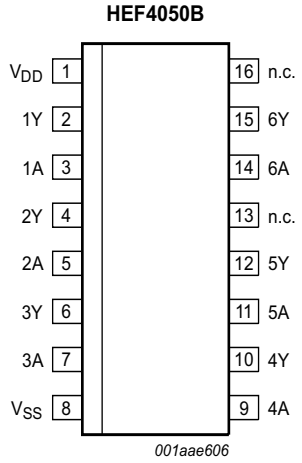



**Fig 4. Pin configuration**

## 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $V_{DD}$ | 1 | supply voltage |
| 1Y to 6Y | 2, 4, 6, 10, 12, 15 | output |
| 1A to 6A | 3, 5, 7, 9, 11, 14, | input |
| $V_{SS}$ | 8 | ground supply voltage |
| n.c. | 13, 16 | not connected |

# 7. Functional description

**Table 3. Guaranteed fan-out**

| Driven element | Guaranteed fan-out |
|---|---|
| Standard TTL | 2 |
| 74 LS | 9 |
| 74 L | 16 |

## 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | –0.5 | +18 | V |
| $I_{IK}$ | input clamping current | $V_I < –0.5$ V | –10 | - | mA |
| $V_I$ | input voltage | | –0.5 | +18 | V |
| $I_{OK}$ | output clamping current | $V_O < –0.5$ V or $V_O > V_{DD} + 0.5$ V | - | ±10 | mA |
| $I_{I/O}$ | input/output current | | - | 10 | mA |
| $I_{DD}$ | supply current | | - | 50 | mA |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $T_{amb}$ | ambient temperature | | –40 | +85 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ –40 °C to +85 °C | | | |
| | | SO16 package [1] | - | 500 | mW |
| P | power dissipation | per output | - | 100 | mW |

[1] For SO16 package: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | 3 | 15 | V |
| $V_I$ | input voltage | | 0 | 15 | V |
| $T_{amb}$ | ambient temperature | in free air | –40 | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD}$ = 5 V | - | 3.75 | µs/V |
| | | $V_{DD}$ = 10 V | - | 0.5 | µs/V |
| | | $V_{DD}$ = 15 V | - | 0.08 | µs/V |

## 10. Static characteristics

**Table 6. Static characteristics**

*$V_{SS}$ = 0 V; $V_I$ = $V_{SS}$ or $V_{DD}$ unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | $T_{amb}$ = –40 °C | | $T_{amb}$ = 25 °C | | $T_{amb}$ = 85 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $\|I_O\| < 1$ µA | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $\|I_O\| < 1$ µA | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | V |

**Table 6. Static characteristics** *...continued*

*$V_{SS}$ = 0 V; $V_I$ = $V_{SS}$ or $V_{DD}$ unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | $T_{amb}$ = –40 °C | | $T_{amb}$ = 25 °C | | $T_{amb}$ = 85 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $V_{OH}$ | HIGH-level output voltage | $\|I_O\|$ < 1 μA | 5 V | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | | 10 V | 9.95 | - | 9.95 | - | 9.95 | - | V |
| | | | 15 V | 14.95 | - | 14.95 | - | 14.95 | - | V |
| $V_{OL}$ | LOW-level output voltage | $\|I_O\|$ < 1 μA | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| $I_{OH}$ | HIGH-level output current | $V_O$ = 2.5 V | 5 V | - | –1.7 | - | –1.4 | - | –1.1 | mA |
| | | $V_O$ = 4.6 V | 5 V | - | –0.52 | - | –0.44 | - | –0.36 | mA |
| | | $V_O$ = 9.5 V | 10 V | - | –1.3 | - | –1.1 | - | –0.9 | mA |
| | | $V_O$ = 13.5 V | 15 V | - | –3.6 | - | –3.0 | - | –2.4 | mA |
| $I_{OL}$ | LOW-level output current | $V_O$ = 0.4 V | 4.75 V | 3.5 | - | 2.9 | - | 2.3 | - | mA |
| | | $V_O$ = 0.5 V | 10 V | 12.0 | - | 10.0 | - | 8.0 | - | mA |
| | | $V_O$ = 1.5 V | 15 V | 24.0 | - | 20.0 | - | 16.0 | - | mA |
| $I_I$ | input leakage current | | 15 V | - | ±0.3 | - | ±0.3 | - | ±1.0 | μA |
| $I_{DD}$ | supply current | $I_O$ = 0 A | 5 V | - | 4.0 | - | 4.0 | - | 30 | μA |
| | | | 10 V | - | 8.0 | - | 8.0 | - | 60 | μA |
| | | | 15 V | - | 16.0 | - | 16.0 | - | 120 | μA |
| $C_I$ | input capacitance | | | - | - | - | 7.5 | - | - | pF |

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

*$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; for test circuit see Figure 6; unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | | Extrapolation formula | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | HIGH to LOW propagation delay | nA to nY; see Figure 5 | 5 V | [1] | 26 ns + (0.18 ns/pF)$C_L$ | - | 35 | 70 | ns |
| | | | 10 V | | 16 ns + (0.08 ns/pF)$C_L$ | - | 20 | 35 | ns |
| | | | 15 V | | 12 ns + (0.05 ns/pF)$C_L$ | - | 15 | 30 | ns |
| $t_{PLH}$ | LOW to HIGH propagation delay | nA to nY; see Figure 5 | 5 V | [1] | 28 ns + (0.55 ns/pF)$C_L$ | - | 55 | 110 | ns |
| | | | 10 V | | 14 ns + (0.23 ns/pF)$C_L$ | - | 25 | 55 | ns |
| | | | 15 V | | 12 ns + (0.16 ns/pF)$C_L$ | - | 20 | 40 | ns |
| $t_{THL}$ | HIGH to LOW output transition time | see Figure 5 | 5 V | [1] | 7 ns + (0.35 ns/pF)$C_L$ | - | 25 | 50 | ns |
| | | | 10 V | | 3 ns + (0.14 ns/pF)$C_L$ | - | 10 | 20 | ns |
| | | | 15 V | | 2 ns + (0.09 ns/pF)$C_L$ | - | 7 | 14 | ns |
| $t_{TLH}$ | LOW to HIGH output transition time | see Figure 5 | 5 V | [1] | 10 ns + (1.00 ns/pF)$C_L$ | - | 60 | 120 | ns |
| | | | 10 V | | 9 ns + (0.42 ns/pF)$C_L$ | - | 30 | 60 | ns |
| | | | 15 V | | 6 ns + (0.28 ns/pF)$C_L$ | - | 20 | 40 | ns |

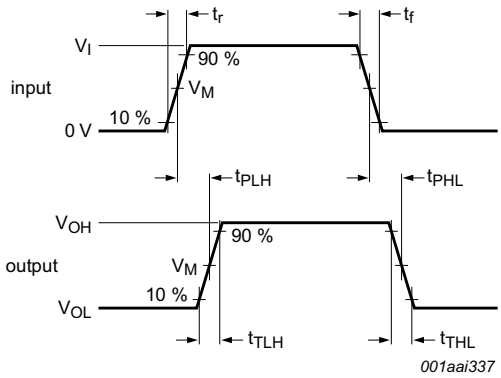
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ($C_L$ in pF).

**Table 8. Dynamic power dissipation $P_D$**

*$P_D$ can be calculated from the formulas shown. $V_{SS}$ = 0 V; $t_r = t_f \leq 20$ ns; $T_{amb}$ = 25 °C.*

| Symbol | Parameter | $V_{DD}$ | Typical formula for $P_D$ (µW) | where: |
|---|---|---|---|---|
| $P_D$ | dynamic power dissipation | 5 V | $P_D = 3800 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $f_i$ = input frequency in MHz, $f_o$ = output frequency in MHz, $C_L$ = output load capacitance in pF, $V_{DD}$ = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs. |
| | | 10 V | $P_D = 11600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |
| | | 15 V | $P_D = 65900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |

## 12. Waveforms



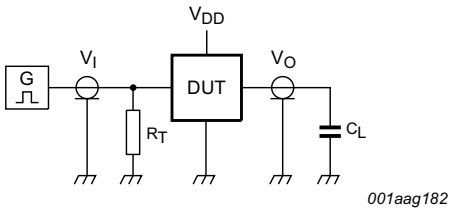

Measurement points are given in Table 9.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 5. Input to output propagation delays**

**Table 9. Measurement points**

| Input | | Output |
|---|---|---|
| $V_M$ | $V_I$ | $V_M$ |
| $0.5V_{DD}$ | 0 V to $V_{DD}$ | $0.5V_{DD}$ |




Test data is given in Table 10.

Definitions for test circuit:

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

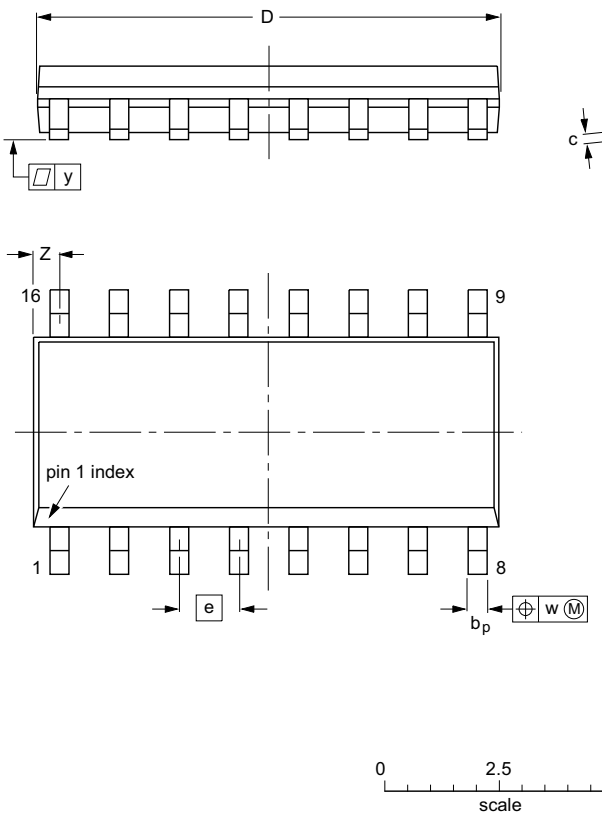
**Fig 6. Test circuit for measuring switching times**

**Table 10. Test data**

| **Supply voltage** | **Input** | | | **Load** |
|---|---|---|---|---|
| **$V_{DD}$** | **$V_I$** | **$V_M$** | **$t_r$, $t_f$** | **$C_L$** |
| 5 V to 15 V | $V_{DD}$ | $0.5V_I$ | ≤ 20 ns | 50 pF |

## 13. Package outline

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**







**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 7. Package outline SOT109-1 (SO16)**

## 14. Abbreviations

**Table 11. Abbreviations**

| Acronym | Description |
|---|---|
| DTL | Diode Transistor Logic |
| DUT | Device Under Test |
| LOCMOS | Local Oxidation CMOS |
| TTL | Transistor-Transistor Logic |

## 15. Revision history

**Table 12. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| HEF4050B v.10 | 20160623 | Product data sheet | - | HEF4050B v.9 |
| Modifications: | • Table 4: condition for input clamping current changed (typo corrected).<br>• Table 5: maximum value for input voltage changed (typo corrected). | | | |
| HEF4050B v.9 | 20160324 | Product data sheet | - | HEF4050B v.8 |
| Modifications: | • Type number HEF4050BP (SOT38-4) removed. | | | |
| HEF4050B v.8 | 20111118 | Product data sheet | - | HEF4050B v.7 |
| Modifications: | • Table 6: $I_{OH}$ minimum values changed to maximum<br>• Table 11: DUT added | | | |
| HEF4050B v.7 | 20091201 | Product data sheet | - | HEF4050B v.6 |
| HEF4050B v.6 | 20090723 | Product data sheet | - | HEF4050B v.5 |
| HEF4050B v.5 | 20081111 | Product data sheet | - | HEF4050B v.4 |
| HEF4050B v.4 | 20080702 | Product data sheet | - | HEF4050B_CNV v.3 |
| HEF4050B_CNV v.3 | 19950101 | Product specification | - | HEF4050B_CNV v.2 |
| HEF4050B_CNV v.2 | 19950101 | Product specification | - | - |

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