LITE-ON SEMICONDUCTOR

T16M5T600B

Sensitive Gate Triacs
Sillicon Bidirectional Thyristors

TRIACS
16 AMPERES RMS
600 VOLTS

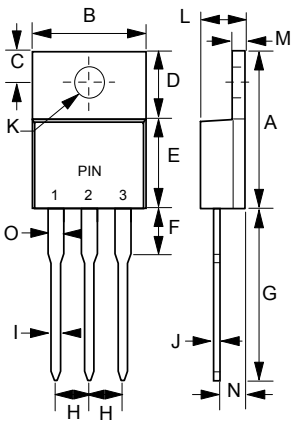
FEATURES

- Sensitive Gate allows Triggering by Microcontrollers and other
- Maximum Values of IGT, VGT and IH Specified for Ease of Design
- On-State Current Rating of 15 A RMS at 70℃
- High Surge Current Capability - 120 A
- Blocking Voltage to 800 V
- Uniform Gate Trigger Currents in Three Quadrants, Q1, Q2, and Q3
- Pb Free Package

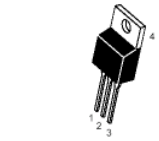
MECHANICAL DATA

- Case: Molded plastic
- Weight: 0.07 ounces, 2.0 grams

TO-220AB



TO-220AB		
DIM.	MIN.	MAX.
A	14.22	15.88
B	9.65	10.67
C	2.54	3.43
D	5.84	6.86
E	8.26	9.28
F	-	6.35
G	12.70	14.73
H	2.29	2.79
I	0.51	1.14
J	0.40	0.67
K	3.53⌀	4.09⌀
L	3.56	4.83
M	1.14	1.40
N	2.03	2.92
O	1.17	1.37
All Dimensions in millimeter		



PIN ASSIGNMENT	
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

MAXIMUM RATINGS (Tj= 25℃ unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak Repetitive Off– State Voltage (1) (TJ= -40 to 110℃, Sine Wave, 50 to 60 Hz; Gate Open)	VDRM, VRRM	600	Volts
On-State RMS Current (TC = +70℃) Full Cycle Sine Wave 50 to 60 Hz	IT(RMS)	16	Amp
Peak Non-Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, TJ= +25℃) Preceded and followed by rated current.	ITSM	120	Amps
Circuit Fusing Consideration (t = 8.3 ms)	I^2t	93	A^2s
Peak Gate Power (TC = +70℃, Tp≦ 1.0 us)	PGM	20	Watt
Average Gate Power (TC = +70℃, t=8.3 ms)	PG(AV)	0.5	Watt
Operating Junction Temperature Range	TJ	-40 to +110	℃
Storage Temperature Range	Tstg	-40 to +150	℃

Notice: (1) VDRM and VRRM for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

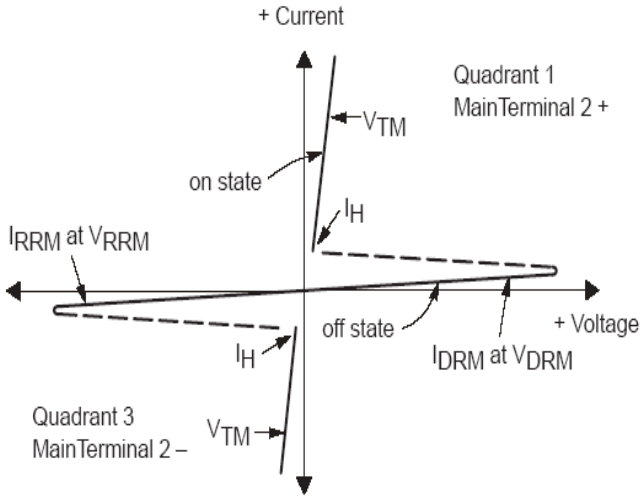
THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance - Junction to Case - Junction to Ambient	R_{thJC} R_{thJA}	2.0 62.5	℃/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	T_L	260	℃

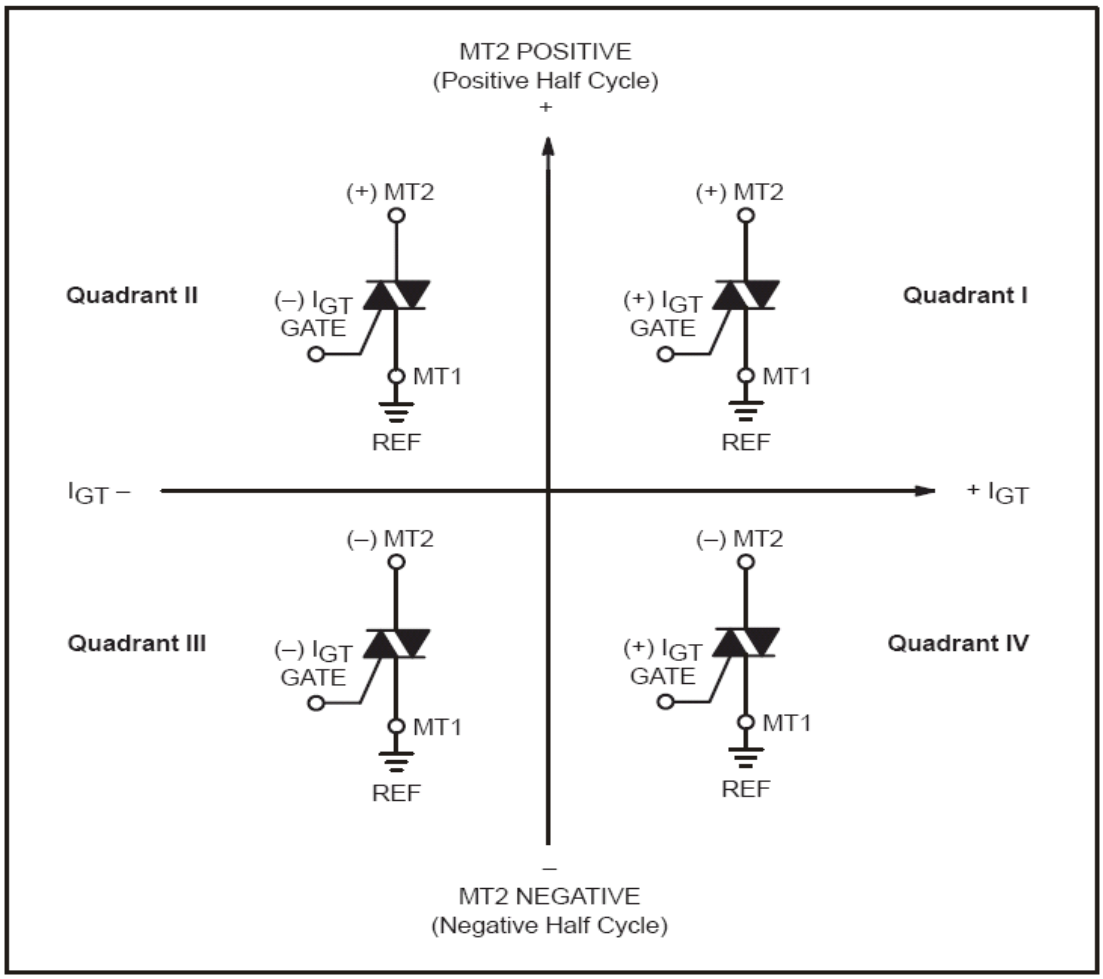
ELECTRICAL CHARACTERISTICS (T_C=25℃ unless otherwise noted, Electrical apply in both directions)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Peak Reptitive Forward or Reverse Blocking Current (T_J=25℃ (V_D=Rated V_{DRM}, V_{RRM}; Gate Open) T_J=110℃	I_{DRM} I_{RRM}	---- ----	---- ----	0.01 2.0	mA
ON CHARACTERISTICS					
Peak On-State Voltage (I_{TM}=± 21 A Peak @Tp ≦ 2.0 ms, Duty Cycle ≦ 2%)	V_{TM}	----	----	1.8	Volts
Gate Trigger Current (V_D = 12Vdc; R_L = 100 Ohms)	I_{GT1} I_{GT2} I_{GT3}	---- ---- ----	2.0 3.0 3.0	5.0 5.0 5.0	mA
Gate Trigger Voltage (V_D = 12 Vdc; R_L =100 Ohms)	V_{GT1} V_{GT2} V_{GT3}	0.45 0.45 0.45	0.62 0.60 0.65	1.5 1.5 1.5	Volts
Holding Current (V_D = 12 V, Initiating Current = ± 150 mA, Gate Open)	I_H	----	3.0	10	mA
Latching Current (V_D = 24 V, I_G = 50 mA)	I_L	---- ---- ----	5.0 10 5.0	15 20 15	mA
DYNAMIC CHARACTERISTICS					
Critical Rate of Change of Commutation Current (V_D = Rated VDRM , I_{TM} = 3.5 A, Commutating dv/dt = 10 V/us, Gate Unenergized,T_C = 110℃,f = 250 Hz,Snubber: Cs = 0.01 uf,Rs =15 Ohms)	di/dt(c)	8.0	10	----	A/ms
Critical Rate of Rise of Commutation Voltage (V_D = 67% V_{DRM} , Exponential Waveform,R_{GK} = 510 Ohms, T_C = 110℃)	dv/dt	25	75	----	V/us

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions



All polarities are referenced to MT1
Whith in -phase signal (using standard AC lines) quadrants I and III are used

Figure 1.RMS Current Derating

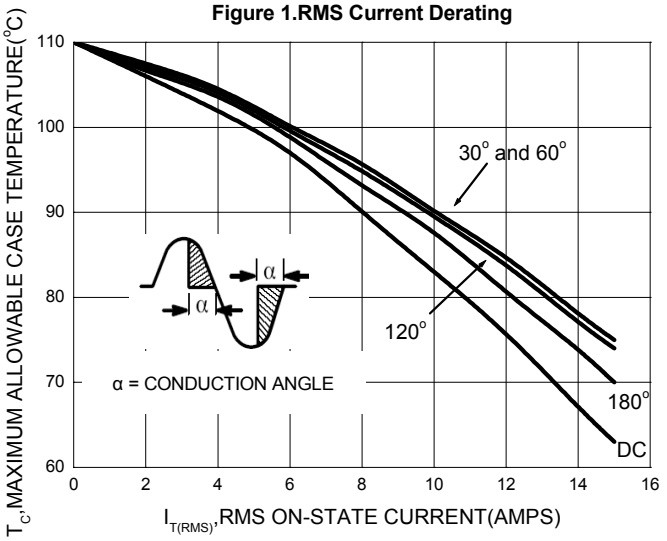


Figure 2. Maximum On-State Power Dissipation

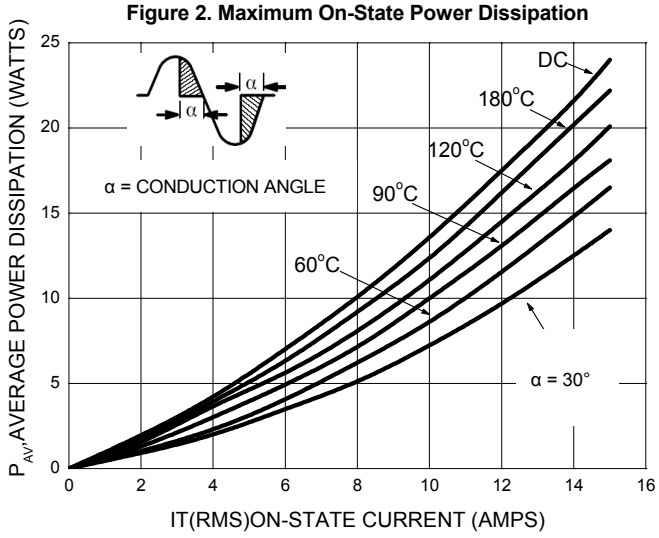
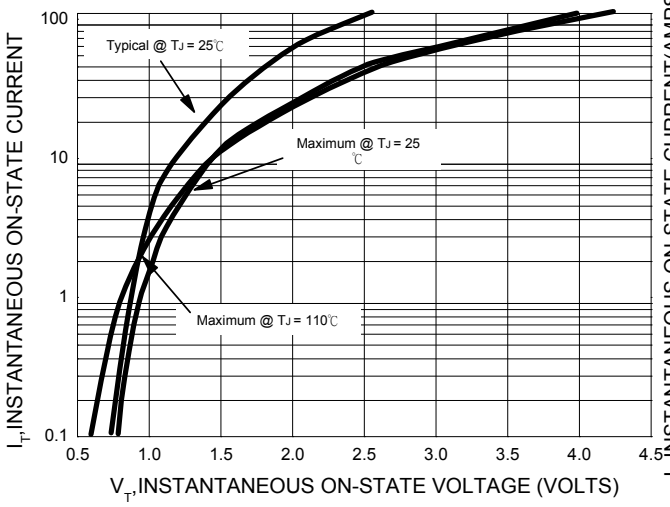


Figure 3. On-State Characteristics



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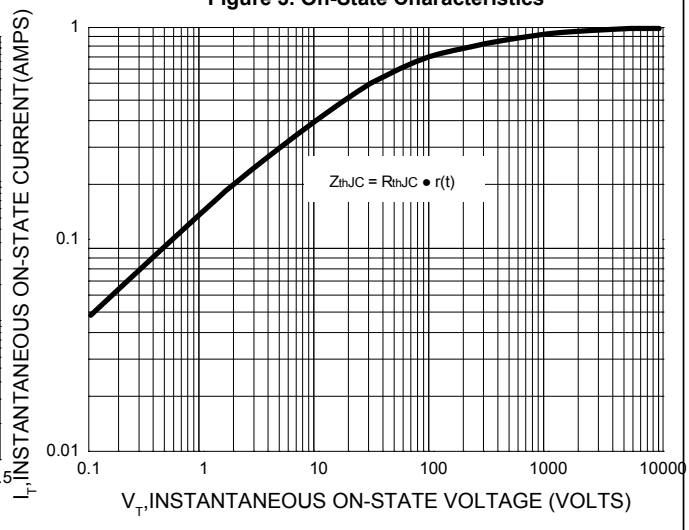


Figure 5. Typical Hold Current Versus Junction Temperature

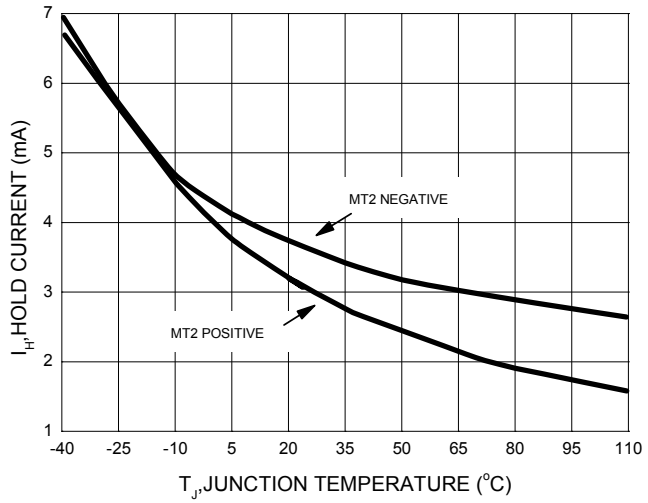


Figure 6. Typical Latching Current Versus Junction Temperature

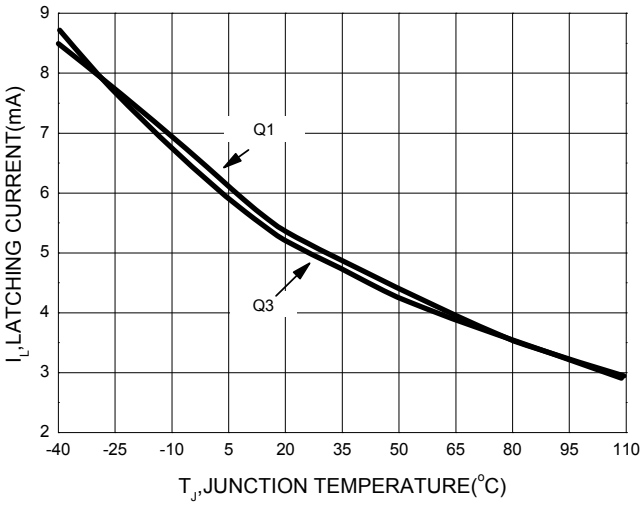


Figure 7.Typical Gate Trigger Current Versus Junction emperature

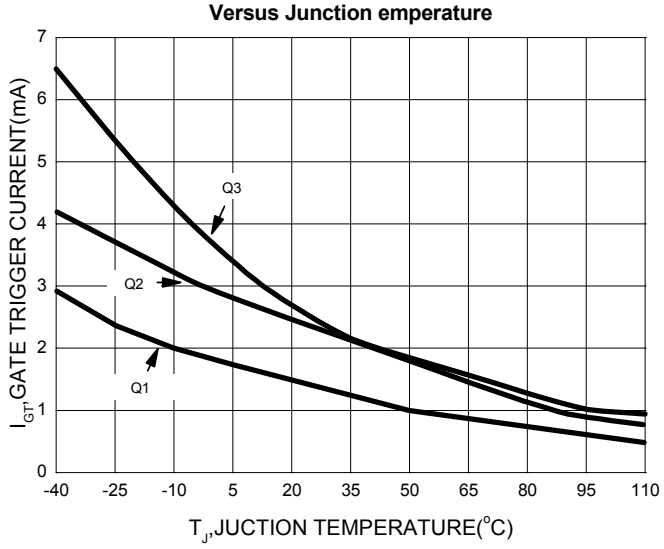


Figure 8.Typical Gate Trigger Voltage Versus Junction Temperature

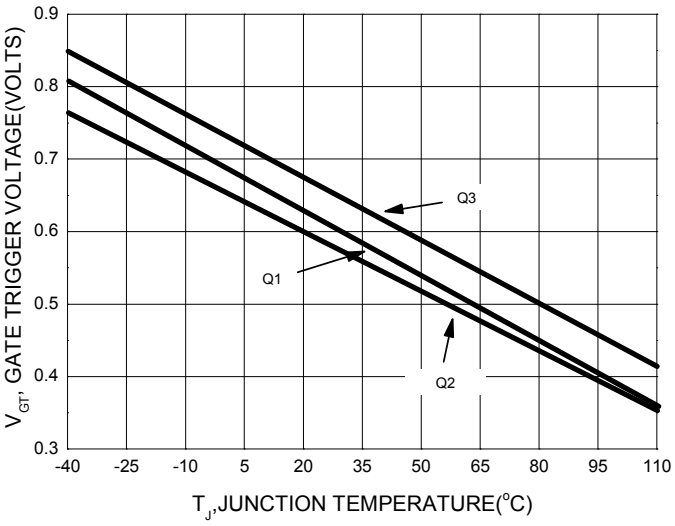


Figure 9. Typical Exponential Static dv/dt Versus Gate-MT1 Resistance, MT2(+)

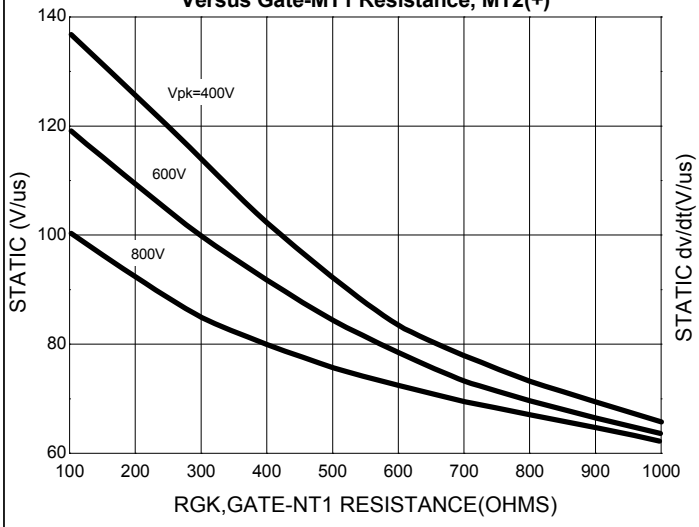


Figure 10. Typical Exponential Static dv/dt Versus Peak Voltage,MT2(+)

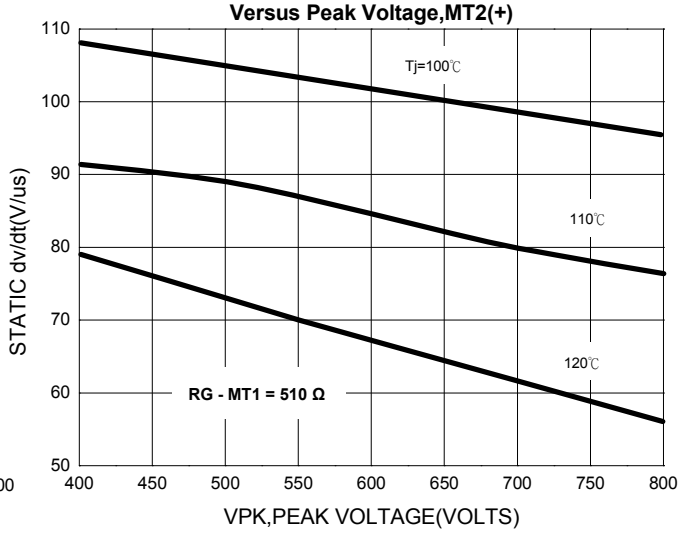


Figure 11. Typical Exponential Static dv/dt Versus Junction Temperature, MT2(+)

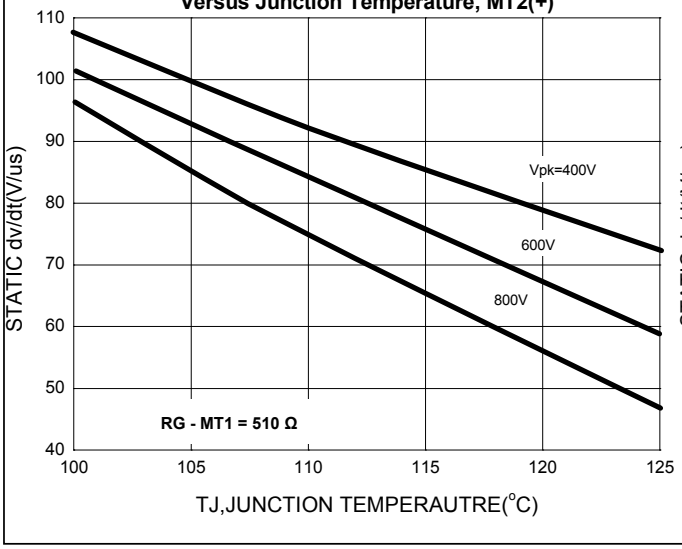


Figure 12. Typical Exponential Static dv/dt Versus Peak Voltage,MT2(-)

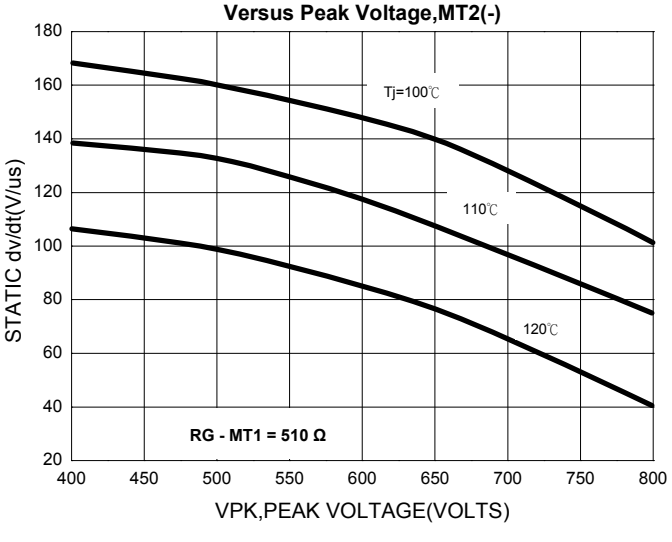


Figure 13. Typical Exponential Static dv/dt Versus Junction Temperature,MT2(-)

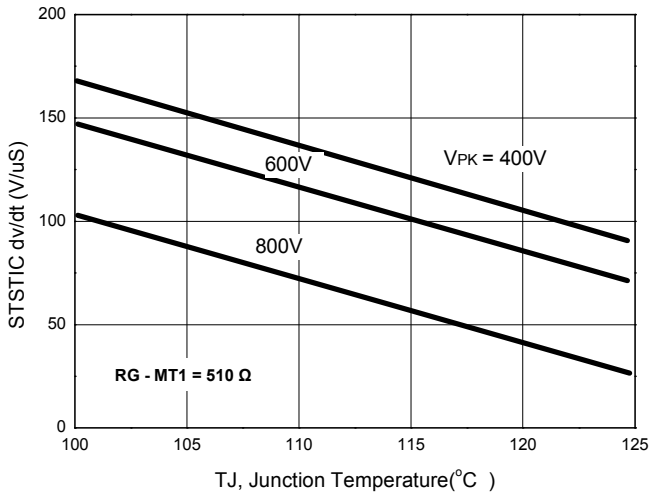
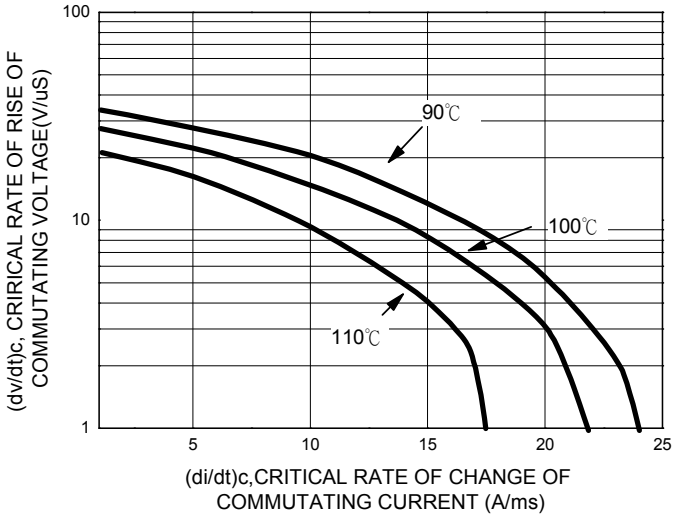


Figure 14. Critical Rate of Rise of Commutating Voltage



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